REMARKS

Applicants respectfully request consideration of this application. The enclosed is responsive to Examiner's Office Action mailed April 25, 2007. Claims 1-12 are pending for examination and have been rejected. Claim 12 has been amended. No new matter has been added as a result of this amendment.

Rejections Under 35 U.S.C. §102/§103

Examiner has rejected claims 1-2, 4-8 and 10-12 under 35 U.S.C. §102(b) as being anticipated by *Maegawa* (U.S. Patent No. 5,578,513). Examiner has rejected claims 2 and 9 under 35 U.S.C. §103(a) as being unpatentable over *Maegawa* in view of *Yu* (U.S. Patent No. 6,475,869).

In claims 1-12, Applicants teach and claim a nonplanar transistor having a gate electrode that fully wraps around the channel region or almost wraps all the way around the channel region.

In one embodiment of the present invention, a two step etch process, which includes an anisotropic etch (Figure 6E) followed by an isotropic etch (Figure 6F), is used to form the gate electrode. The anisotropic etch defines the gate electrode and the isotropic etch removes gate electrode material from regions underneath the semiconductor body 620 so that undesired "stringers" are not left which can short the source and drain regions to the gate electrode. The two step etch process illustrated in Figures 6E and 6F forms a gate electrode where the bottom portion laterally undercuts the top portion as illustrated in Figures 6F and claimed by applicant in claims 1-6.

It is Applicants' understanding that *Maegawa* fails to disclose a gate electrode where the bottom portion laterally undercuts the top portion as claimed by Applicants in claims 1-6. Applicants understand *Maegawa* to disclose, in each of the embodiments, a gate electrode where

the bottom portion and the top portion have the same dimensions. Indeed, *Maegawa* makes no distinction between the bottom portion and the top portion of a gate electrode because the entire gate electrode is the same width.

Furthermore, in other embodiments of the present invention, the gate electrode is formed with a replacement gate process. In such a process a dielectric film is formed over and around the semiconductor body and an opening is formed in the dielectric film to expose the semiconductor body. The use of an isotropic etch results in an opening 705 formed in the insulating substrate that is wider than the opening 704 formed in the dielectric film.

In this process, a portion of the insulating substrate is removed using an isotropic etch to undercut and expose at least a portion of the bottom surface of the semiconductor body (Figures 7B and 8F). After forming a gate dielectric layer on the top surface and sidewalls of the semiconductor body as well as on the exposed portion of the bottom surface, a gate electrode material is blanket deposited over the dielectric film and into the opening (Figures 7C and 8G). In one embodiment, the dielectric film 702 is then removed from the top surface of the dielectric film to define the gate electrode (Figure 7D). The resulting gate electrode (of embodiments depicted in Figures 7D and 8G) has a top portion above the insulating substrate and a bottom portion formed in the insulating substrate wherein the bottom portion is wider than the top portion as claimed in claims 7-12.

It is Applicants' understanding that *Maegawa* fails to disclose a gate electrode that has a top portion above an insulating substrate and a bottom portion formed in the insulating substrate wherein the bottom portion is wider than the top portion as claimed in claims 7-12. It is Applicants' understanding that *Maegawa* discloses in every one of the embodiments a gate

electrode where the bottom portion and the top portion have the same dimensions as discussed *supra*.

Applicants respectfully submit that *Maegawa* does not disclose each and every element as claimed by Applicants and fails to teach or render obvious Applicants' invention as claimed in claims 1-12. In the Office Action, Examiner notes that "the amended claims fail to overcome all embodiments taught by the prior art reference of *Maegawa* as shown in the present Office Action" (O.A. ¶12). Applicants submit that Examiner has not pointed out how or where the embodiments in the prior art references teach the "laterally undercut" and the "wider" limitations as claimed in claims 1 and 7 respectively. Applicants assert that *Maegawa* alone or in combination with any secondary reference does not teach or render obvious the "laterally undercut" and the "wider" limitations as claimed in claims 1 and 7 respectively. Accordingly, Applicants respectfully request the removal of the 35 U.S.C. §§102 and 103 rejections of claims 1-12.

Double Patenting

Claim 12 has been objected to under 37 C.F.R. §1.75 as being a substantial duplicate of claim 6. Applicants have amended claim 12 to depend on claim 7, and accordingly, claim 12 is patentably distinct from claim 6. Thus, Applicants respectfully request the removal of the objection of claim 12.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully submit that the applicable rejections and objections have been overcome. Applicants respectfully submit that the present application and all pending claims are in condition for allowance.

Pursuant to 37 C.F.R. §1.136(a)(3), Applicants hereby request and authorize the U.S. Patent and Trademark Office to treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time, and to charge all required fees, including extension of time fees and fees under 37 C.F.R. §§1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully Submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 7/25/07

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